**LISTING OF THE CLAIMS**

1. (original) A processor comprising:

a heat release frequency holding unit which holds a heat release frequency of a plurality of blocks subject to heat release control;

a heat release identifying unit which identifies a block involved in the execution of each execution unit comprising at least one instruction, and which identifies a heat release coefficient related to a heat value of the identified block; and

a heat release frequency adder unit which cumulatively increases, for each execution unit, the heat release frequency of the identified block by referring to the heat release coefficient, as the execution of instructions proceeds.

2. (original) The processor according to claim 1, wherein the heat release identifying unit is a decoder for decoding instructions to be executed.

3. (original) The processor according to claim 1, further comprising a heat release frequency subtractor unit which subtracts from the heat release frequency of the blocks in accordance with heat discharge that occurs with time.

4. (original) The processor according to claim 3, wherein the heat release frequency subtractor unit subtracts such that the larger the heat release frequency of the operational block, the larger the amount of subtraction.

5-8. (cancelled)

9. (original) A multiprocessor system including a plurality of subprocessors and a main processor, wherein the main processor comprises:

a heat release frequency holding register which holds a heat release frequency of a plurality of blocks in each of the subprocessors;

a heat release identifying unit which identifies a block involved in the execution of each execution unit comprising at least one instruction, and which identifies a heat release coefficient related to a heat value of the identified block;

a heat release frequency adder unit which cumulatively increases, for each execution unit, the heat release frequency of the identified block by referring to the heat release coefficient, as the execution of instructions proceeds; and

a scheduler which allocates instructions to be executed among the plurality of subprocessors in accordance with the heat release frequency of the blocks.

10-19. (cancelled)

20. (original) A processor system comprising:

a heat release frequency holding unit which holds a heat release frequency of a plurality of blocks subject to heat release control;

a heat release identifying unit which identifies a block involved in the execution of each execution unit comprising at least one instruction, and which identifies a heat release coefficient related to a heat value of the identified block; and

a heat release frequency adder unit which cumulatively increases, for each execution unit, the heat release frequency of the identified block by referring to the heat release coefficient, as the execution of instructions proceeds.

21-23. (cancelled)

24. (original) An information processing apparatus comprising:

a heat release frequency holding unit which holds a heat release frequency of a plurality of blocks subject to heat release control;

a heat release identifying unit which identifies a block involved in the execution of each execution unit comprising at least one instruction, and which identifies a heat release coefficient related to a heat value of the identified block; and

a heat release frequency adder unit which cumulatively increases, for each execution unit, the heat release frequency of the identified block by referring to the heat release coefficient, as the execution of instructions proceeds.

25-27. (cancelled)